

Final Exam Model Answer Subject: Microprocessor Systems - ECE 311C **Date:** Mon 26/12/2016 **Duration:** 3 hours

№ of Questions: 3 in 5 page(s) **Total Points:** 90 تخلفات

Question 1: [10 Points] Describe the special uses for each of the following registers.

EAX: Accumulator register. Used in arithmetic operations Accumulator for operands and results

EDX: Data register. Used in arithmetic operations and I/O operations

ESP: Stack Pointer register. Pointer to the top of the stack

ESI: Source register. Used as a pointer to a source in stream and array operations

EIP: Instruction Pointer

Question 2:

[20 Points]

Put $\boldsymbol{\sqrt{}}$ in front of correct statement and X in front of wrong one

No	Statement	Answer
1.	The DI registers is a 16-bit register.	\checkmark
2.	The register SI is divided to two registers each of 8 bits.	Х
3.	Data transfer instructions can affect the flag bits.	Х
4.	The registers SP/ESP are used with CS register to locate the next instruction.	Х
5.	Displacement is a signed value, so it can be both positive and negative.	√
6.	In real mode, a far jump accesses any location within the first 1M byte by changing both CS and IP.	√

8.	In real-mode addressing if the beginning segment address is 028FH the memory location having an effective address of 03FFFH lies within the segment.	\checkmark
9.	The maximum size of memory segment is 640K bytes of memory.	Х
10.	The combinations (DS:BX) locates the next instruction executed by the microprocessor.	Х

Question 3:

[60 Points]

Identify the choice that best completes the statement or answers the question.

- **1.** If **ES = D321H**, then the range of physical addresses for the **extra segment** is:
 - a) 00000H 0D321H c) <mark>D3210H E320FH</mark>
 - b) D3210H D321FH d) 0D321H 1D320H
- 2. If **CS** = **020AH**, **SS** = **0801H**, **SI** = **0100H** and **IP** = **1BCDH** the address of the next instruction is:
 - a) <mark>03C6D</mark>
 - b) 03D5D d) None of the above
- **3.** Which of the following defines a constant **Count**?
 - a) Count db 80 c) mov Count, 80
 - b) Count equ 80 d) None of them

Assume the following same initial processor state to answer questions (4), (5), and (6) below. Treat each part individually.

AX	6521 H
BX	ABCD H
СХ	0105 H
DX	876F H

Flags					
С	Α	Ζ	S	Р	0
1	0	1	0	0	0

c) 03C70

4. What will be the contents of **AX** after **SUB AL**, **AH**

a) <mark>65BC H</mark>	c) BC21 H
b) 4421 H	d) 6544 H

5. What are the **flags** after **CMPAH**, **CL**

	a) C=1, Z=0, S=1	c) C=0, Z=1, S=1
	b) C=0, Z=1, S=0	d) C=0, Z=0, S=0
6. What are the contents of BL after OR BL , 1FH		, 1FH
	a) DF H	c) FC H
	b) D2 H	d) DD H

7	Which of the following is an illegal 8086	instruction?			
	a) add ax. [cx]	c) mov ax. [bx]			
	b) inc [si]	d) add by [by]			
8	The instruction mov ax. [sil is an example	of			
0.	a) indexed addressing	c) direct addressing			
	b) indirect addressing	d) based addressing			
9	The instruction PUSH AI .	a) bused dual cooling			
0.	a) Decrement SP by 2 and push a word	to stack			
	b) Increment SP by 2 and push a word	to stack			
	c) Decrement SP by 1 and push a AI, to stack				
	d) Illegal				
10.	can be used as indexed i	registers in real addressing mode .			
	a) BX, SI, DI	c) AX, SI, DI			
	b) SI, DI, DS	d) AX, BX, CX			
11.	What will be the final value of ax ?	, , ,			
	mov ax, 6				
	mov ecx, 4				
	L1:				
	inc ax				
loop L1					
	loop L1				
	loop L1 a) 11	<mark>c) 10</mark>			
	loop L1 a) 11 b) 9	<mark>c) 10</mark> d) None of the above			
12.	 loop L1 a) 11 b) 9 .Let X1 be an array of words, one of the formula of the	 c) 10 d) None of the above b) b) b			
12.	 loop L1 a) 11 b) 9 .Let X1 be an array of words, one of the forfitth element in X1 to FF 	 c) 10 d) None of the above ollowing is a correct code to set the 			
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c) CX	d) BX		
18. One of the following memory models is used for MS DOS Applications only:			
a) Tiny	c) Small		
b) Medium	d) Flat		
19. The offset of a particular segment varies :	from:		
a) 000H to FFFH	c) 0000H to FFFFH		
b) 00H to FFH	d) 00000H to FFFFFH		
20. The conditional branch instruction JNS pe	erforms the operations when if		
a) <mark>SF=0</mark>	c) ZF=0		
b) PF=0	d) CF=0		
21. The instruction TEST is most similar to			
a) AND	c) OR		
b) XOR	d) NOT		
22. What values of AX and BX will cause the	following jump to occur:		
CMP BX, AX			
JG THERE			
a) AX=2345H, BX=1234H	c) AX=0002H, BX=C000H		
b) $AX = BX$	d) AX=C000H, BX=0002H		
23.Memory segmentation (partitioning) was	s necessary because the x86 registers		
were 16-bits and could not hold the 20-bit	addresses of the main memory		
a) True	b) False		
24. In real mode, a far jump accesses any loc	ration within the first 1M byte by		
changing both CS and IP .			
a) True	b) False		
25. A 20-bit address bus allows access to a m	nemory of capacity		
	c) 32MB		
b) 2 MB	d) 64 MB		
26. In the Intel architecture, there are actually several buses connecting the CPU to			
the rest of the computer. Which of the following is not such a bus ?			
a) The control bus	c) The data bus		
b) The logic bus	d) The address bus		
27. Which flags are NOT used for mathemat	ical operations?		
a) Carry, Interrupt and Trap flag			
b) Direction, Interrupt and Sign flag			
c) Direction, Overflow and Trap flag			
d) Direction, Interrupt and Trap flag			
28. The bus that defines the " size " of the proc	essor is		

a) The system bus

b) <mark>The data bus</mark>

c) The address bus

d) The control bus

29.If **DS = 90A3H**, then the range of **physical addresses** for the data segment is:

a) 90A30H – 9FA30H

c) 090A3 – 190A2H

b) 00000H – 090A3H

d) 90A30 – A0A2FH

30.The **read/write** line is

- a) belongs to the address bus
- b) CPU bus
- c) belongs to the control bus
- d) belongs to the data bus