Question 1:
Describe the special uses for each of the following registers.
EAX: Accumulator register. Used in arithmetic operations Accumulator for operands and results

EDX: Data register. Used in arithmetic operations and I/O operations

ESP: Stack Pointer register. Pointer to the top of the stack

ESI: Source register. Used as a pointer to a source in stream and array operations

EIP: Instruction Pointer

Question 2:
[20 Points]
Put $\sqrt{ }$ in front of correct statement and $X$ in front of wrong one

| No | Statement | Answer |
| :---: | :---: | :---: |
| 1. | The DI registers is a 16-bit register. | $\checkmark$ |
| 2. | The register SI is divided to two registers each of 8 bits. | $X$ |
| 3. | Data transfer instructions can affect the flag bits. | $X$ |
| 4. | The registers SP/ESP are used with CS register to locate the next instruction. | $X$ |
| 5. | Displacement is a signed value, so it can be both positive and negative. | $\checkmark$ |
| 6. | In real mode, a far jump accesses any location within the first 1M byte by changing both CS and IP. | $\checkmark$ |


| 8. | In real-mode addressing if the beginning segment address <br> is $028 F H$ the memory location having an effective address <br> of $03 F F F H$ lies within the segment. | $V$ |
| :---: | :--- | :---: |
| 9. | The maximum size of memory segment is 640 K bytes of <br> memory. | $X$ |
| 10. | The combinations (DS:BX) locates the next instruction <br> executed by the microprocessor. | $X$ |

Question 3:
[60 Points]
Identify the choice that best completes the statement or answers the question.

1. If $\mathbf{E S}=\mathbf{D} 321 \mathbf{H}$, then the range of physical addresses for the extra segment is:
a) $00000 \mathrm{H}-0 \mathrm{D} 321 \mathrm{H}$
c) $\mathbf{D} 3210 \mathrm{H}$ - E320FH
b) D3210H - D321FH
d) $0 \mathrm{D} 321 \mathrm{H}-1 \mathrm{D} 320 \mathrm{H}$
2. If $\mathbf{C S}=\mathbf{0 2 0 A H}, \mathbf{S S}=\mathbf{0 8 0 1 H}, \mathbf{S I}=\mathbf{0 1 0 0 H}$ and $\mathbf{I P}=\mathbf{1 B C D H}$ the address of the next instruction is:
a) 03 C 6 D
c) $\mathbf{0 3 C 7 0}$
b) 03 D 5 D
d) None of the above
3. Which of the following defines a constant Count?
a) Count db 80
c) mov Count, 80
b) Count equ 80
d) None of them

Assume the following same initial processor state to answer questions (4), (5), and (6) below. Treat each part individually.

| AX | 6521 H |
| :--- | :--- |
| BX | ABCD H |
| CX | 0105 H |
| DX | 876 F H |


| Flags |  |  |  |  |  |
| :--- | :--- | :--- | :--- | :--- | :--- |
| $\mathbf{C}$ | $\mathbf{A}$ | $\mathbf{Z}$ | $\mathbf{S}$ | $\mathbf{P}$ | $\mathbf{O}$ |
| $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{0}$ | $\mathbf{0}$ |

4. What will be the contents of AX after SUB AL, AH
a) 65 BC H
b) $\mathbf{4 4 2 1 \mathrm { H }}$
c) BC 21 H
d) 6544 H
5. What are the flags after CMP AH, CL
a) $\mathrm{C}=1, \mathrm{Z}=0, \mathrm{~S}=1$
b) $\mathrm{C}=0, \mathrm{Z}=1, \mathrm{~S}=0$
c) $\mathrm{C}=0, \mathrm{Z}=1, \mathrm{~S}=1$
d) $\mathrm{C}=0, \mathrm{Z}=0, \mathrm{~S}=0$
6. What are the contents of $\mathbf{B L}$ after OR BL, 1FH
a) DF H
b) $\mathbf{D} 2 \mathrm{H}$
c) FCH
d) DD H
7. Which of the following is an illegal 8086 instruction?
a) add ax, [cx]
c) $\operatorname{mov} a x,[b x]$
b) inc [si]
d) add bx, [bx]
8. The instruction $\mathbf{m o v} \mathbf{a x},[\mathbf{s i}]$ is an example of
a) indexed addressing
c) direct addressing
b) indirect addressing
d) based addressing
9. The instruction PUSH AL
a) Decrement SP by 2 and push a word to stack
b) Increment SP by 2 and push a word to stack
c) Decrement SP by 1 and push a AL to stack
d) Illegal
10. $\qquad$ can be used as indexed registers in real addressing mode.
a) BX, SI, DI
c) AX, SI, DI
b) SI, DI, DS
d) $\mathbf{A X}, \mathrm{BX}, \mathrm{CX}$
11. What will be the final value of ax?
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mov ax, 6
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mov ecx, 4

## L1:

inc ax
$\operatorname{loop} \mathrm{L} 1$
a) 11
c) 10
b) 9
d) None of the above
12. Let $\mathbf{X 1}$ be an array of words, one of the following is a correct code to set the fifth element in X1 to FF
a) $\operatorname{movX1}+5, \mathrm{Ffh}$
b) $\operatorname{mov} \mathrm{X} 1+4, \mathrm{Ffh}$
c) $\operatorname{movX1}+10, \mathrm{Ffh}$
d) $\operatorname{mov} \mathrm{X} 1+8, \mathrm{Ffh}$
13. Which mode does Windows use?
a) Real mode
b) Protected mode
14. Which of the following is an invalid instruction?
a) MOV AX, [BP]
c) MOV AX, CS
b) MOV DS, CS
d) None of the above
15. Which of the following is not an MASM directive?
a) .Data
c) DWORD
b) RET
d) .MODEL
16. The call instruction is used to
a) access subprograms
c) perform I/O
b) access memory
d) access the Stack
17. Which of the following is not a general purpose register?
a) $\mathbf{A X}$
b) CS
c) CX
d) $\mathbf{B X}$
18. One of the following memory models is used for MS DOS Applications only:
a) Tiny
c) Small
b) Medium
d) Flat
19.The offset of a particular segment varies from $\qquad$ :
a) $\mathbf{0 0 0 H}$ to $\mathbf{F F F H}$
b) $\mathbf{0 0 H}$ to $\mathbf{F F H}$
c) $\mathbf{0 0 0 0 H}$ to FFFFH
d) $\mathbf{0 0 0 0 0 H}$ to FFFFFH
20. The conditional branch instruction JNS performs the operations when if
a) $\mathrm{SF}=0$
b) $\mathbf{P F}=\mathbf{0}$
c) $\mathbf{Z F}=\mathbf{0}$
d) $\mathrm{CF}=0$
21.The instruction TEST is most similar to----------
a) AND
c) OR
b) XOR
d) NOT
22. What values of $\mathbf{A X}$ and $\mathbf{B X}$ will cause the following jump to occur:

CMP BX, AX
JG THERE
a) $\mathrm{AX}=2345 \mathrm{H}, \mathrm{BX}=1234 \mathrm{H}$
b) $\mathbf{A X}=\mathbf{B X}$
c) $\mathrm{AX}=0002 \mathrm{H}, \mathrm{BX}=\mathrm{C} 000 \mathrm{H}$
d) $\mathrm{AX}=\mathbf{C 0 0 0 H}, \mathrm{BX}=0002 \mathrm{H}$
23. Memory segmentation (partitioning) was necessary because the $x 86$ registers were 16-bits and could not hold the 20-bit addresses of the main memory
a) True
b) False
24. In real mode, a far jump accesses any location within the first $\mathbf{1} \mathbf{M}$ byte by changing both CS and IP.
a) True
b) False
25.A 20-bit address bus allows access to a memory of capacity
a) 1 MB
b) $\mathbf{2 ~ M B}$
c) 32 MB
d) $\mathbf{6 4 ~ M B}$
26.In the Intel architecture, there are actually several buses connecting the CPU to the rest of the computer. Which of the following is not such a bus?
a) The control bus
c) The data bus
b) The logic bus
d) The address bus
27. Which flags are NOT used for mathematical operations?
a) Carry, Interrupt and Trap flag
b) Direction, Interrupt and Sign flag
c) Direction, Overflow and Trap flag
d) Direction, Interrupt and Trap flag
28. The bus that defines the "size" of the processor is $\qquad$
a) The system bus
b) The data bus
c) The address bus
d) The control bus
29.If $\mathbf{D S}=\mathbf{9 0 A} \mathbf{3 H}$, then the range of physical addresses for the data segment is:
a) $90 \mathrm{~A} 30 \mathrm{H}-9 \mathrm{FA} 30 \mathrm{H}$
b) $00000 \mathrm{H}-090 \mathrm{~A} 3 \mathrm{H}$
c) $090 \mathrm{~A} 3-190 \mathrm{~A} 2 \mathrm{H}$
d) $90 \mathrm{~A} 30-\mathrm{A} 0 \mathrm{~A} 2 \mathrm{FH}$
30.The read/write line is
a) belongs to the address bus
b) CPU bus
c) belongs to the control bus
d) belongs to the data bus

